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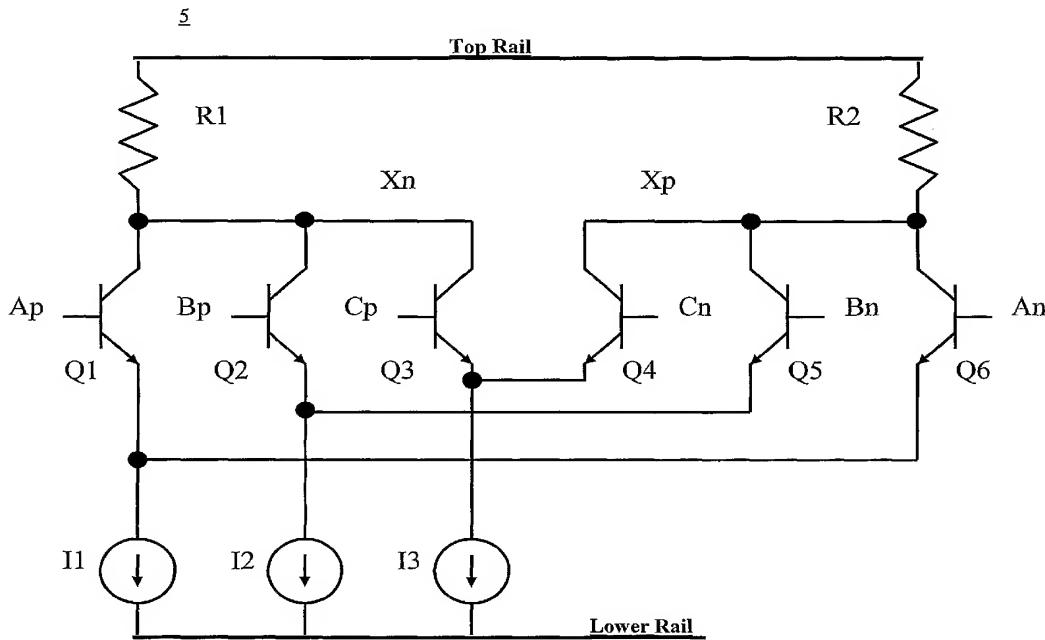
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[Continued on next page]

(54) Title: SINGLE-LEVEL PARALLEL-GATED CARRY/MAJORITY CIRCUITS AND SYSTEMS THEREFROM



(57) Abstract: A carry/majority circuit, comprising a plurality of differential transistor pairs coupled in parallel and forming a pair of output nodes, with a single parallel gated level. Current is steered through a leg of the transistor pair having a higher input voltage.

WO 2006/012362 A2



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